What is Claimed:

1. A circuit for driving a dual-gated MOSFET, said dual-gated MOSFET being switchable between conduction and blocking modes, said dual-gated MOSFET having a shielding gate, a switching gate, a gate-to-drain overlap region, and a drain-to-source resistance when the MOSFET is in the conduction mode, said circuit comprising:

means for generating a first voltage signal for driving said shielding gate, said first voltage signal having a first voltage level for charging the gate-to-drain overlap region and a fourth voltage level for reducing the drain-to-source resistance when the MOSFET is in the conduction mode;

means for generating a second voltage signal for driving the switching gate, said second voltage signal being switchable between a low and a high voltage level; and

control means for controlling each of said means for generating to thereby switch the MOSFET between the conduction and blocking modes.

2. The circuit of claim 1, wherein said control means causes said means for generating a first voltage signal to maintain said first voltage signal at said first voltage level or bring said first voltage signal to said first voltage level at a predetermined amount of time prior to switching the MOSFET from the blocking to the conduction mode.

3. The circuit of claim 2, wherein said control means causes said means for generating said second voltage signal to be switched from said low to said high voltage level

thereby causing the MOSFET to enter the conduction mode, and at a first delay time thereafter causes said first voltage signal to be switched from said first voltage level for charging the gate-to-drain overlap region to said fourth voltage level for reducing the drain-to-source resistance while the MOSFET is in the conduction mode.

4. The circuit of claim 2, wherein said control means causes said means for generating said first voltage signal to be switched from said fourth voltage level for reducing the drain-to-source resistance to said first voltage level for charging the gate-to-drain overlap region or to ground potential, and at a second delay time thereafter causes said second voltage signal to be switched from said high voltage level to said low voltage level.

5. The circuit of claim 2, wherein said first voltage level for charging the gate-to-drain overlap region is from approximately three to approximately six volts.

6. The circuit of claim 2, wherein said fourth voltage level for reducing the drain-to-source resistance is from approximately nine to approximately thirteen volts.

7. The circuit of claim 2, wherein said low voltage level of said second voltage signal is one of approximately zero volts and approximately ground potential.

8. A method for driving a dual-gated MOSFET, the dual-gated MOSFET being switchable between conduction and blocking modes, the dual-gated MOSFET having a

shielding gate, a switching gate, a gate-to-drain overlap region, and a drain-to-source resistance when the MOSFET is in the conduction mode, said method comprising:

applying a first voltage signal to the shielding gate;

maintaining the first voltage signal at a first voltage level prior to switching the MOSFET from the blocking mode to the conduction mode, the first voltage level being selected to substantially completely charge the gate-to-drain overlap region of the MOSFET; and

further applying a second voltage signal to the switching gate, the second voltage signal switching the MOSFET between the blocking and conduction modes.

9. The method of claim 8, wherein said maintaining step comprises one of continuously maintaining the first voltage signal at the first voltage level and maintaining the first voltage signal at the first voltage level for a predetermined amount of time prior to switching the MOSFET from the blocking to the conduction mode.

10. The method of claim 8, wherein said further applying step comprises switching the second voltage signal from a low voltage level to a high voltage level to thereby place the MOSFET in the conduction mode.

11. The method of claim 10, further comprising the steps of:

delaying a first delay time after the further applying step; and

changing the first voltage signal from the first voltage level selected to substantially completely charge the gate-to-drain overlap region of the MOSFET to a fourth voltage level selected to reduce the resistance between the drain and source of the MOSFET while in the conduction mode.

12. The method of claim 11, wherein said first delay time comprises the rise time of the switching gate.

13. The method of claim 11, further comprising the steps of:

returning the first voltage signal from the fourth voltage level selected to reduce the resistance between the drain and source of the MOSFET while in the conduction mode to one of the first voltage level selected to substantially completely charge the gate-to-drain overlap region of the MOSFET or ground potential;

delaying a second delay time; and

further returning the second voltage signal from the high voltage level to the low voltage level to a thereby place the MOSFET in the blocking mode.

14. The method of claim 13, wherein said second delay time comprises the fall time of the shielding gate.

15. A method of driving a dual-gated MOSFET, the dual-gated MOSFET having a shielding gate, a switching gate, a Miller capacitance between the MOSFET gate and drain,

and a drain-to-source resistance when the MOSFET is in the conduction mode, said method comprising:

preparing the MOSFET to switch from the blocking mode to the conduction mode by applying a first voltage signal at a first voltage level to the shielding gate, the first voltage level being selected to substantially completely charge the Miller capacitance and thereby reduce switching losses; and

applying a second voltage signal to the switching gate to switch the MOSFET between the blocking and conduction modes.

16. The method of claim 15, further comprising:

delaying a first delay time following said applying step; and

changing the first voltage signal to a fourth voltage level selected to substantially reduce the resistance between the drain and source of the MOSFET to thereby reduce conduction losses.

17. The method of claim 16, wherein said first delay time comprises the rise time of the switching gate.

18. The method of claim 16, further comprising the step of returning the first voltage signal to the first voltage level to thereby substantially completely discharge the Miller capacitance thereby preparing the MOSFET to switch from the conduction mode to the blocking mode.

19. The method of claim 18, further comprising the steps of:

further delaying a second delay time following said returning step; and

switching said second voltage signal to said low voltage level.

20. The method of claim 15, wherein said preparing step comprises one of continuously maintaining the first voltage signal at the first voltage level or maintaining the first voltage signal at the first voltage level for a predetermined amount of time prior to switching the MOSFET from the blocking to the conduction mode.

21. The method of claim 15, wherein said preparing step comprises one of continuously maintaining the first voltage signal at the first voltage level or maintaining the first voltage signal at the first voltage level for a predetermined amount of time prior to switching the MOSFET from the blocking to the conduction mode.